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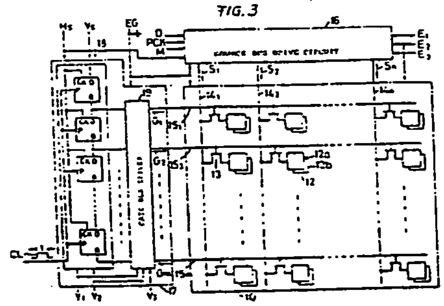
(54) METHOD OF ERASING LIQUID CRYSTAL DISPLAY AND AN ERASING CIRCUIT.

(57) When the display is to be erased from active matrix-type liquid crystal display elements which have a source bus drive circuit (16) and a gate bus drive circuit (17), pixel signals for turning the pixels off are supplied in an amount of one line to the source bus drive circuit and, at the same time, a clear signal (CL) is given to a gate bus drive circuit (17) to apply a voltage simultaneously to all gate buses (15_1 to 15_m) to turn on the transistors (13) in all of the pixels. Provision is made of a power source holding circuit (22) for holding the power of the power source (V_1) supplied to the gate bus drive circuit (17) for a predetermined period of time even after the power source is turned off, and a voltage drop detect circuit (24) for detecting the turn-off of the power source. A clear signal (CL) is produced in response to the detect signal and is sent to the gate bus drive circuit (17). In response to the clear signal, the gate bus drive circuit supplies a voltage for turning on the transistors (13) of all pixels simultaneously to all of the gate buses to erase the display in a short period of time after the power source is turned off.

FIG. 3



EP 0 364 590 A1

S P E C I F I C A T I O N

TITLE OF THE INVENTION

METHOD AND CIRCUIT FOR ERASING A LIQUID CRYSTAL DISPLAY

TECHNICAL FIELD

The present invention relates to a method and a circuit for erasing a display of an active matrix type liquid crystal display cell having a capacitive storage effect.

TECHNICAL BACKGROUND

A brief description will be given first, with reference to Fig. 1, of a typical prior art active matrix type liquid crystal display cell which has a capacitive storage effect. Fig. 1 shows a liquid crystal display panel 10 in which display pixels 12 are arranged in the form of a matrix (with m rows and n columns) and their display electrodes 12a are connected to drains of TFTs (Thin Film Transistors) 13, respectively. The TFTs 13 have their sources and gates connected to those of perpendicularly intersecting source buses 14_1 to 14_n and gate buses 15 which correspond to them, respectively. The display pixels 12 each include a counter electrode (also referred to as a common electrode) 12b disposed opposite the display electrode 12a.

A source bus drive circuit 16 is provided for driving the source buses 14_1 through 14_n. From a main body (not shown) of the liquid crystal display device the source bus drive circuit is supplied with a pixel clock PCK, a horizontal synchronizing signal Hs and a control signal M for converting the power supply

voltage into an AC form, such as shown in Fig. 2, and pixel data (a binary code representing logic "1" or "0") D which is applied in the horizontal direction in synchronism with the pixel clock PCK, though not shown. In the source bus drive circuit 16 the pixel data D of one row are sequentially loaded into a shift register 16a in synchronism with the pixel clock PCK, and in correspondence to the pixel data D, signals S_1 to S_n to be displayed on the pixels of one row of the liquid crystal display panel 10 are simultaneously provided on the source buses 4_1 to 4_n upon each occurrence of the horizontal synchronizing signal Hs. The signals S_1 to S_n are also called source bus drive signals, and they have voltages E_1 and E_2 (in the case of a field $M = 1$) or E_3 and E_4 (in the case of a field $M = 0$) depending upon the logic "1" and "0" of the pixel data D, as shown in Fig. 2D in which one signal S_j is exemplified. Here, $E_2 = (E_1 + E_3)/2$. The source bus drive circuit 16 operates on the DC voltages E_1, E_2 and E_3 and a common potential EG (zero volt) from the main body of the liquid crystal display device.

The liquid crystal display panel 10 is also supplied with the common potential EG from the main body of the display device and the counter electrodes of the respective pixels are each supplied with a voltage corresponding to the voltage E_2. The common potential EG (zero volt) and the voltages E_1, E_2 and E_3 are selected such that $E_1 > EG > E_2 > E_3$, for instance.

A gate bus drive circuit 17 drives the gate buses 15_1 to 15_m high-level one after another upon each occurrence of the horizontal synchronizing signal Hs, thereby turning ON the TFTs of one row from the first to the mth row in a sequential order. As a result of

this, the source bus drive signals S_1 to S_n are applied to the corresponding pixels, respectively. The gate bus drive circuit is made up principally of an m-stage shift register 18 and a gate bus driver 19. A vertical synchronizing signal Vs (Fig. 2E) is applied, as a start signal, to a data terminal D of the first-stage shift register, and the horizontal synchronizing signal Hs is applied to a clock terminal CK of each stage. Pulses, which result from sequential delaying of the start signal for the horizontal synchronizing signal period, are provided from output terminals Q of the respective stages to the gate bus driver 19. In the gate bus driver 19 the input pulses are converted in level, providing on the gate buses 15_1 to 15_m gate bus drive signals G_1 to G_m (Fig. 2F) each of which has a voltage level V_1 or V_3 depending on whether the input pulse from the corresponding stage is high- or low-level. From the main body of the device the power supply voltages V_1 and V_2 are supplied to the shift register 18 and the gate bus driver 19 and the power supply voltage V_3 is supplied to the gate bus driver 19. These voltages are selected such that $V_1 > V_2 > V_3$, and in many cases, $V_1 - V_2 = 5$ volts.

To clear a display at a desired time, pixel data for one field (m rows) which have logic "0" for erasing displays of respective pixels are provided from the main body of the device, and upon each occurrence of the horizontal synchronizing signal Hs, voltage E_2 signals for m rows are simultaneously applied from the source bus drive circuit 16 to the source buses 14_1 through 14_n and the gate buses 15_1 through 15_m are sequentially driven high-level by the gate bus driver 17, whereby the display of one field is cleared. That

is, clearing of one field display needs a time mT_H (where T_H is the cycle of the horizontal synchronizing signal) at the shortest. This is not preferable because, for example, when the liquid crystal display panel 10 is used with a computer, the higher the display-clearing frequency, the longer the time for which the computer is occupied.

To stop the display device from the display operation, it is customary to turn OFF the power supply switch of the display device main body without involving any particular display clearing operation mentioned above. Upon turning OFF the switch, various signals provided to the liquid crystal display panel disappear and various power supply voltages also drop to the common potential (the ground potential) within a short time. The output G_i of the gate bus driver also disappears and drops to the common potential. Consequently, all the TFTs 13 of the liquid crystal display panel 10 are turned OFF, and charges stored in pixel capacitances remain undischarged for a relatively long period of time, because their external discharge paths are cut off. This allows residual images to remain on the display screen, impairing the display quality. Furthermore, to leave the pixels stored with charges as mentioned above means that DC voltage remains unremoved from the liquid crystal, shortening its life and lowering its reliability.

An object of the present invention is to provide a liquid crystal display erasing method which permits clearing of a display on a liquid crystal display panel in a markedly shorter time than in the past.

Another object of the present invention is to provide a liquid crystal display erasing circuit

which permits clearing of a residual image in a short time upon turning OFF the power supply of a display device and prevents shortening of liquid crystal and lowering of its reliability.

DISCLOSURE OF THE INVENTION

According to the present invention, in the case of clearing a display image on a liquid crystal display panel, pixel data for clearing the display, corresponding to display elements of one row, is applied to a source bus drive circuit, by which all source buses are simultaneously driven to the voltage level corresponding to the above-mentioned pixel data for a predetermined period of time, during which all outputs of a gate bus drive circuit are simultaneously held at an active level by an erasing signal.

Furthermore, according to the present invention, a power holding circuit is provided for holding power of the operating power supply to the gate bus drive circuit for a predetermined period of time after turning OFF of the power supply of the display device. Moreover, means is provided for detecting the turning OFF of the power supply of the display device, and by its detecting signal, the outputs of the gate bus drive circuit are simultaneously held at the active level for a predetermined period of time.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram for explaining the arrangement of conventional active matrix type liquid crystal display elements;

Fig. 2 is a waveform diagram for explaining the operation of the display elements shown in Fig. 1;

Fig. 3 is a diagram illustrating the arrangement of liquid crystal display elements embodying the liquid crystal display erasing method of the present invention;

Fig. 4 is a block diagram illustrating a modified form of a gate bus drive circuit 17 in Fig. 3;

Fig. 5 is a block diagram illustrating a display erasing circuit according to another embodiment of the present invention; and

Fig. 6 is a voltage waveform diagram for explaining the operation of the erasing circuit depicted in Fig. 5.

BEST MODE FOR CARRYING OUT THE INVENTION

In Fig. 3 there is shown an embodiment of the present invention as being applied to the liquid crystal display elements of Fig. 1, the parts corresponding to those in Fig. 1 are identified by the same reference numerals and no detailed description will be given of them. The source bus drive circuit 16 and the liquid crystal display panel 10 are identical with those in Fig. 1. In the embodiment of Fig. 3, the shift register 18 in the gate bus drive circuit 17 is made up of cascade-connected presettable D-type flip-flops, which are adapted so that their preset terminals P can be supplied with a clear signal CL at the same time. The clear signal CL is created in accordance with an operator's instruction or under control of a program in a computer connected to the display device. According to the present invention, in the case of clearing a display image, pixel data D of logic "0" for clearing the display, corresponding to one row of the display panel 10, is provided to the source bus drive circuit 16, from which source bus drive signals

S_1 through S_n of voltage corresponding to the above-mentioned pixel data, i.e. voltage E_2 equal to the voltage of the common electrodes 12b, are simultaneously applied to the source buses 14_1 through 14_n within one horizontal synchronization cycle. In synchronization with this, the clear signal CL is provided to the preset terminal P of each stage of the shift register 18 in the gate bus drive circuit 17 as depicted in Fig. 3. The duration T of the clear signal CL needs only to be equal to or longer than one cycle of the horizontal synchronizing signal Hs. Upon application of the clear signal Hs, the Q output of each stage of the shift register 18 goes to a high level for the time T and the outputs G_1 through G_m of the gate bus driver 19 also go to the high level. (In general, this level needs only to be high enough to activate the TFTs 13 of the liquid crystal display panel 10.) Thus all the TFTs 13 are simultaneously rendered ON during the time T. Consequently, the source bus drive signals S_1 through S_n for clearing the display are supplied to all pixels with m rows and n columns, by which display images are cleared all at once within the time T.

Fig. 4 illustrates another embodiment of the present invention, in which an OR circuit 20 is provided between the shift register 18 and the gate bus driver 19 in the gate bus drive circuit 17 in Fig. 1. Each OR gate of the OR circuit 20 is supplied at one input with the output of the corresponding stage of the shift register 18 and at the other input with the clear signal CL, and the output of each OR gate is applied to the gate bus driver 19. The gate bus driver 19 yields high-level signals G_1 through G_m all at once during the duration T of the input clear signal CL.

Consequently, display images can be cleared all over the display screen within one cycle of the horizontal synchronizing signal Hs as is the case with the embodiment shown in Fig. 3. The source bus drive circuit 16 and the display panel 10 are identical with those in Fig. 1, and hence are not shown.

Fig. 5 illustrates another embodiment of the present invention in which the clear signal CL in the embodiment of Fig. 1 is produced upon turning OFF of the power supply of the display device main body. The source bus drive circuit 16 and the liquid crystal display panel 10 are identical with those in Fig. 1, and hence are not shown.

In this embodiment, as shown in Fig. 5, when the liquid crystal display elements are in operation, that is, when the power supply of the display device main body is ON, a large-capacity capacitor 22b is charged via a diode 22a with the power supply voltage V_1 (which is the same as the voltage V_1 in the prior art example depicted in Fig. 1) which is applied from the liquid crystal display device main body to a terminal 21, and at the same time, the voltage V_1 is provided to the gate bus drive circuit 17. The diode 22a and the capacitor 22b constitute a power holding circuit 22 which holds and supplies power to a load for a predetermined period of time after turning OFF of the power supply of the display device main body. If it is disadvantageous that the output voltage V_1' of the power holding circuit drops below the input voltage V_1, it is also possible to increase the input voltage V_1 in compensation for the voltage drop or provide a DC-DC converter at the input side of the power holding circuit 22 for boosting the input voltage. The output

of the power holding circuit 22 is also applied to a power circuit 23, wherein a voltage V_2' is created as a substitute for the source voltage V_2 which is supplied from the device main body in the prior art, and the voltage V_2' is provided to the gate bus drive circuit 17. Other voltages are the same as those used in the prior art example. That is, the gate bus drive circuit 17 is supplied with the voltage V_3 (which is a low-level voltage of the gate bus drive signal G_i and is used to turn OFF the TFT 13), and though not shown, the source bus drive circuit 16 is supplied with voltages E_1, E_2 and E_3 from the display device main body and the counter electrodes 12b of the liquid crystal display panel 10 are supplied with the voltage E_2. The supply of these voltages V_1, V_3, E_1, E_2 and E_3 is stopped when the power supply of the display device main body is turned OFF.

Now, assuming that the power switch of the display device main body is turned OFF at a time t_1, the voltage V_1 drops to the zero volt (the common potential) at a time t_3 (Fig. 6A). Yet the output voltage V_1' of the power holding circuit 22 gradually decreases with a large time constant $C_{22}R_L$ (where C_{22} is the capacitance of the capacitor 22b and R_L is the load resistance of the power holding circuit 22) (Fig. 6C). On the other hand, the voltage drop of the voltage V_1 is detected by a voltage drop detector 24, and at a time point t_2 when the voltage V_1 has dipped, for instance, 20% below a reference value, the voltage drop detector 24 changes to a low level its output V_B held at a high level until then (Fig. 6B). The output V_B of the voltage drop detector 24 is applied to the output side of the power holding circuit 22 via a capacitor 25 and a resistor 26. The junction F between the

capacitor 25 and the resistor 26 is connected to an input terminal of an inverter 27. The voltage V_F at the junction F drops at the time t_2 and then gradually approaches, with a time constant CR (where C and R are the capacitance of the capacitor 25 and the resistance of the resistor 26, respectively), the output voltage V_1' of the power holding circuit 22 (Fig. 6C).

To the inverter 27 are applied, as its operating voltages, the voltages V_1' and V_2'. After the time point t_2 the voltage V_2' also drops to the common potential with a gradually decreasing time constant, together with the voltage V_1'. Since the threshold level V_{th} of the inverter 27 is set to a level intermediated between the voltages V_1' and V_2' as depicted in Fig. 6C, the inverter 27 yields a high-level output V_{CL} as the clear signal for a period of time T (t_2-t_4) during which the input voltage V_F to the inverter 27 is lower than the threshold level V_{th} (Fig. 6D). The waveform of the output V_{CL} from the inverter 27 is substantially the same as that of the voltage V_1' in the time interval between t_2 and t_4 but is nearly equal to the waveform of the voltage V_2' except that time interval. The pulse width T of the output clear signal CL from the inverter 27 is set to a value a little greater than the time during which the voltages E_1, E_2, V_1 and V_3 supplied to the liquid crystal display panel drop to the common potential when the power supply is turned OFF. That is, $T > (t_3-t_3)$.

The output clear signal CL from the inverter 27 is applied to the preset terminal P of each stage of the shift register 18, and the Q output from each stage is rendered high-level (nearly equal to the voltage V_1') during the time T, and consequently, the outputs

G_1 through G_m of the gate bus driver 19 are also made high-level (which level needs only to be high enough to activate or turn ON the TFTs 13, substantially equal to the voltage V_1' in this instance). All the TFTs 13 of the liquid crystal display panel 10 described previously in conjunction with the prior art example are simultaneously turned ON during the time T, and consequently, the display electrode 12a of each pixel 12 is electrically connected via the TFT to the source bus driver 16b. The source bus driver 16b is arranged so that the potential at its output terminal goes to the common potential EG at substantially the same time as the operating voltages E_1, E_2 and E_3 drop to the common potential. That is, the source bus driver is designed so that the source bus driver signals S_1 through S_n drop to the common potential within the time T. The display electrode 12a and the counter electrode 12b (the latter being supplied with the voltage E_2) are both supplied with the common potential within the time T, and charges stored in each pixel capacitance in accordance with the display being provided are entirely discharged by the end of the time T. In other words, the time T includes the time necessary for discharging the charges stored in the pixel capacitances.

It is evident that the gate bus drive circuit 17 in Fig. 5 may also be replaced with the circuit shown in Fig. 4. While the source bus drive circuit 16 in Fig. 3 has been described to drive the source buses 14_1 through 14_n in such a manner as to provide a binary or ON-OFF display in response to a binary pixel signal as is the case with the prior art example shown in Fig. 1, it is also easy for those skilled in the art to construct the source bus drive circuit 16 so that a

half tone display may be provided using an analog video signal which has a half tone pixel level.

As described above, according to the present invention, display images can be cleared within one cycle of the horizontal synchronizing signal, which is as short as 1/m (where m is the number of rows forming the display screen) of the one-field time needed in the past. Consequently, the display panel of the invention, when used as a display of a computer, is very advantageous in that the time for which the computer is occupied for clearing display images can be reduced accordingly.

Moreover, according to the present invention, the turning OFF of the power supply of the liquid crystal display device is automatically detected and the detection signal is used to hold the TFTs of the liquid crystal display elements in the ON stage for a predetermined period of time so that charges stored in the pixel capacitances can be discharged in a short time. This ensures clearing of residual images in a short time and prevents the reduction of the life of the liquid crystal and lowering of its reliability.

CLAIM

1. A method for erasing a display on an active matrix type liquid crystal display which displays an image by driving source buses in accordance with pixel signals supplied to a source bus drive circuit and selectively driving gate buses one after another through a gate bus drive circuit, comprising:

a step in which pixel signals for turning OFF displays of respective pixels of one row of the matrix display are provided to said source bus drive circuit;

a step in which voltages corresponding to said pixel signals of one row are simultaneously provided to said source buses for a predetermined period of time; and

a step in which a clear signal is generated and applied to said gate bus drive circuit for said predetermined period of time and all of said gate buses are simultaneously held at an active level during the application of said clear signal.

2. A method for erasing a display on an active matrix type liquid crystal display which displays an image by driving source buses in accordance with pixel signals supplied to a source bus drive circuit and selectively driving gate buses one after another through a gate bus drive circuit,

wherein when the power supply of the display is ON, an operating voltage is applied therefrom directly to said source bus drive circuit and an operating voltage is applied via a power holding circuit to said gate bus drive circuit; and

wherein when said power supply is turned OFF, the source voltage is applied to said gate bus drive

circuit from said power holding circuit for a predetermined period of time, and at the same time, the turning OFF of said power supply and a clear signal is generated and applied to said gate bus drive circuit for said predetermined period of time, thereby holding all of said gate buses at an active level for a fixed period of time.

3. A liquid crystal display erasing circuit for erasing a display on a liquid crystal display which includes an active type matrix liquid crystal display panel having transistors respectively connected to pixels arranged in a matrix form, a source bus drive circuit which operates on a source voltage from the power supply of the display and drives source buses connected to the sources of said transistors of respective columns, and a gate bus drive circuit for driving gate buses connected to the gates of said transistors of respective rows; comprising:

power holding means which is supplied with the source voltage from said power supply and holds power for a predetermined period of time after said power supply is turned OFF, said gate bus drive circuit being supplied with an operating voltage via said power holding means from said power supply;

clear signal generating means which detects the turning OFF of said power supply and generates a clear signal; and

all gate bus select means which supplies said clear signal to said gate bus drive circuit for said predetermined period of time, causing said gate bus drive circuit to simultaneously supply all of said gate buses with a voltage for turning ON said transistors.

4. The liquid crystal display erasing circuit

of claim 3, wherein said gate bus drive circuit includes a shift register comprised of a plurality of cascade-connected D-type flip-flops and shifting one stable state along said flip-flops in synchronization with a horizontal synchronizing signal, and a plurality of gate drivers for driving said gate buses in accordance with the outputs from respective output stages of said shift register, and wherein said all gate bus select means is a means which is connected in common to preset terminals of said D-type flip-flops and responds to said clear signal to simultaneously preset all of said D-type flip-flops.

5. The liquid crystal display erasing circuit of claim 3, wherein said gate bus drive circuit includes a shift register composed of a plurality of cascade-connected D-type flip-flops and shifting one stable state along said flip-flops in synchronization with a horizontal synchronizing signal, and a plurality of gate drivers for driving said gate buses in accordance with the outputs from respective output stages of said shift register, and wherein said all gate bus select means is a means which is connected to the inputs of said gate drivers and simultaneously applies said clear signal to all of said gate drivers.

6. The liquid crystal display erasing circuit of claim 4 or 5, wherein said power holding means includes a diode which is connected in its forward direction to said power supply, and a capacitor which is connected to the cathode of said diode and stores a fixed amount of power which is supplied from said power supply.

7. The liquid crystal display erasing circuit of claim 4 or 5, wherein said clear signal generating means includes voltage drop detecting means for detecting

a drop of voltage which is supplied from said power supply, and means which receives, as its operating voltage, the output voltage from said power holding means and generates said clear signal for a substantially fixed period of time after the voltage drop detected by said voltage drop detecting means.

FIG. 1

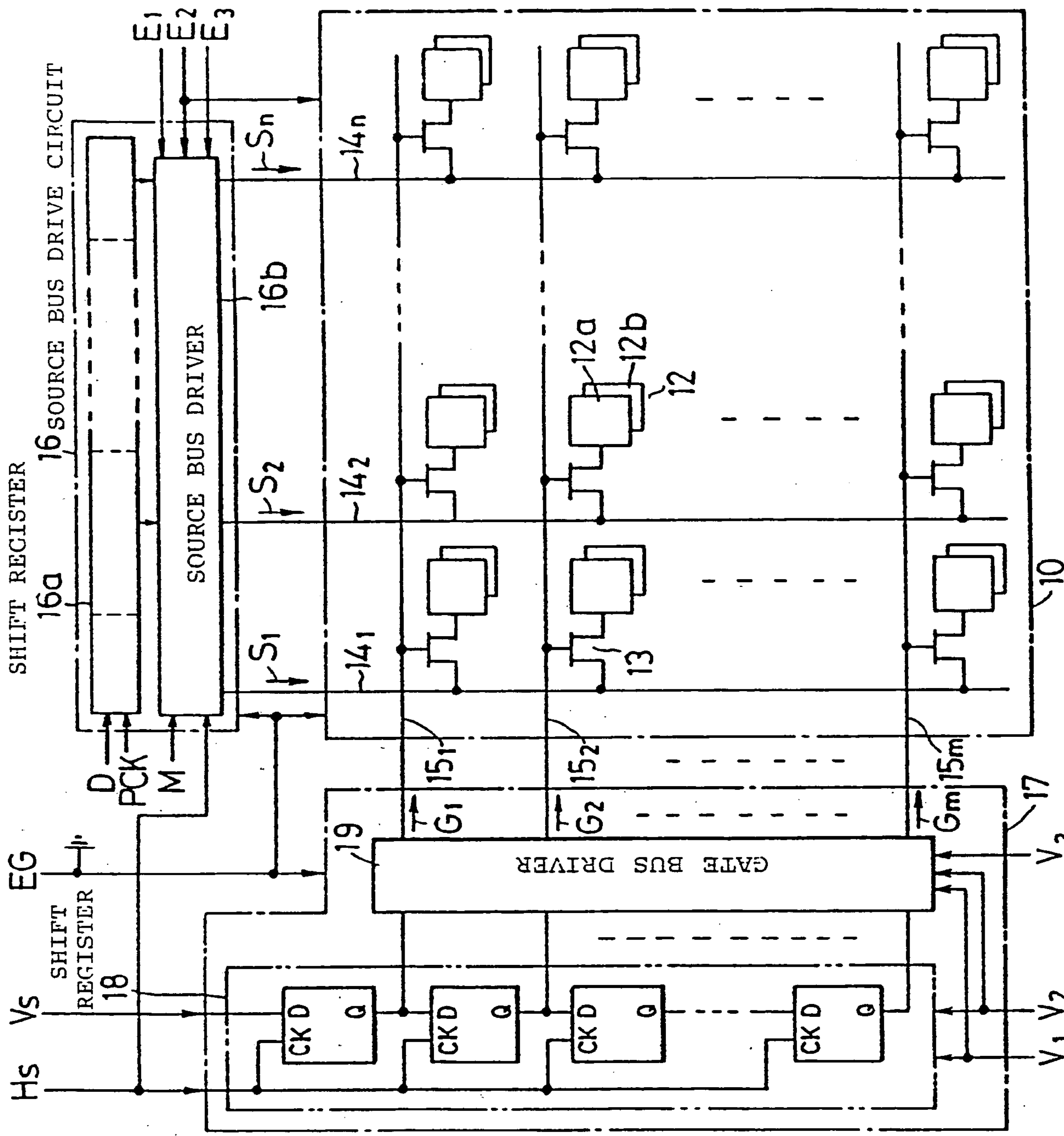

SHIFT REGISTER
16a
16
SOURCE BUS DRIVE CIRCUIT
SOURCE BUS DRIVER
16b
E1
E2
E3
S1
S2
Sn
14₁
14₂
14n
12a
12b
12
13
10
15₁
15₂
15m
D
PCK
M
EG
19
G1
G2
Gm
17
GATE BUS DRIVER
V3
SHIFT REGISTER
18
Vs
Hs
CK D
Q
V1
V2

FIG. 2

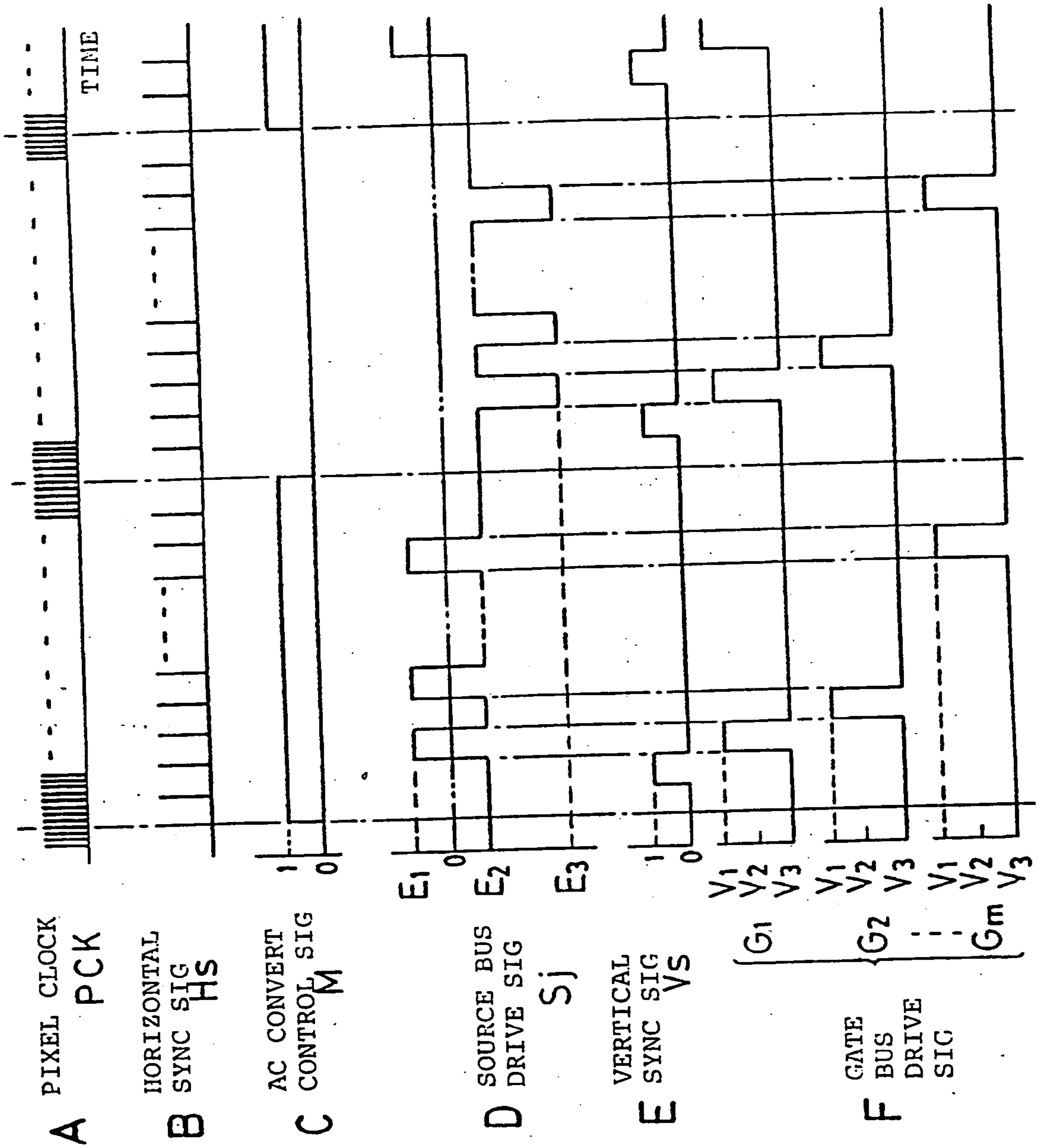

A PIXEL CLOCK PCK
B HORIZONTAL SYNC SIG Hs
C AC CONVERT CONTROL SIG M
D SOURCE BUS DRIVE SIG Sj
E VERTICAL SYNC SIG Vs
F GATE BUS DRIVE SIG
G1
G2
Gm
V1
V2
V3
E1
E2
E3
0
1
TIME

FIG. 3

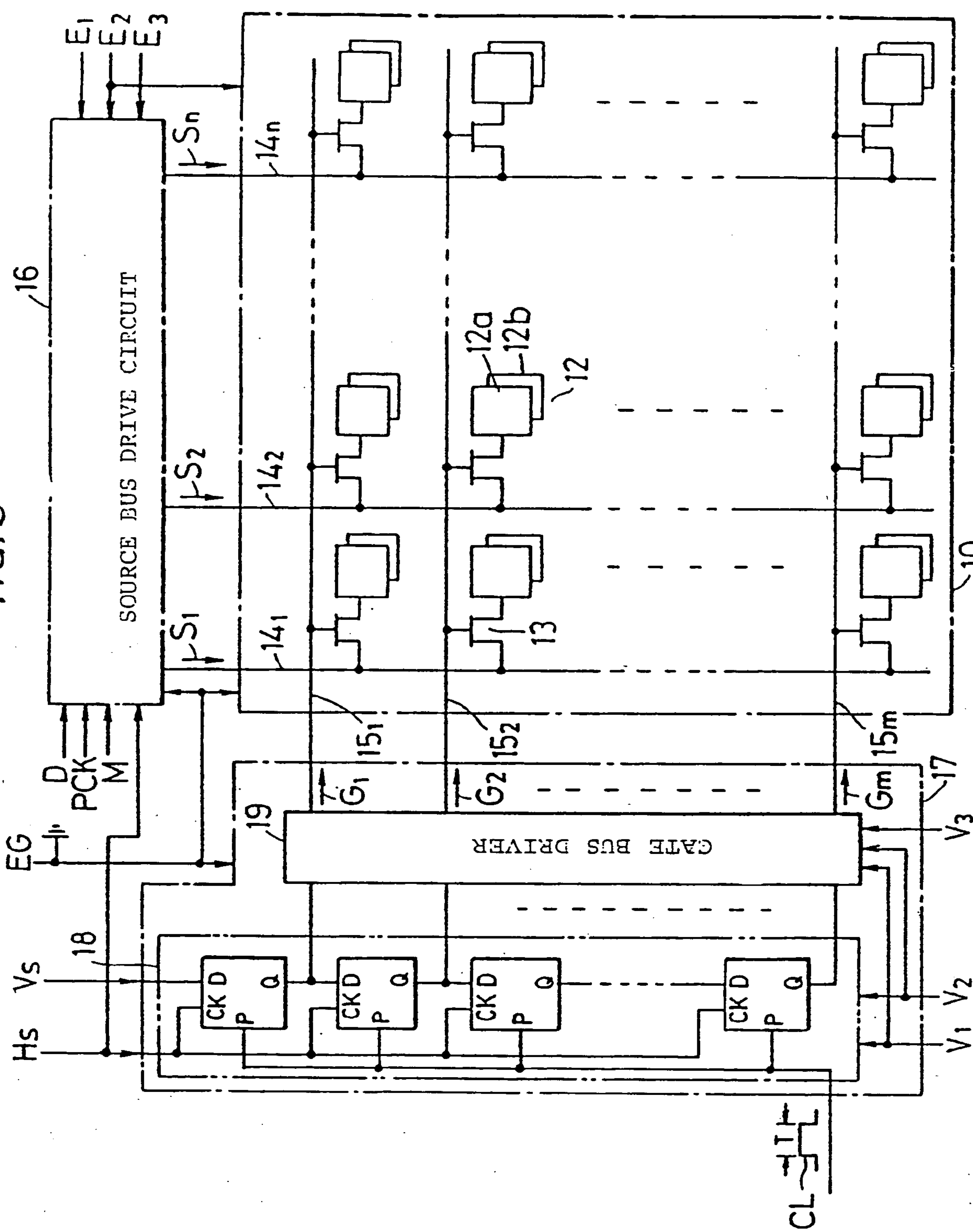
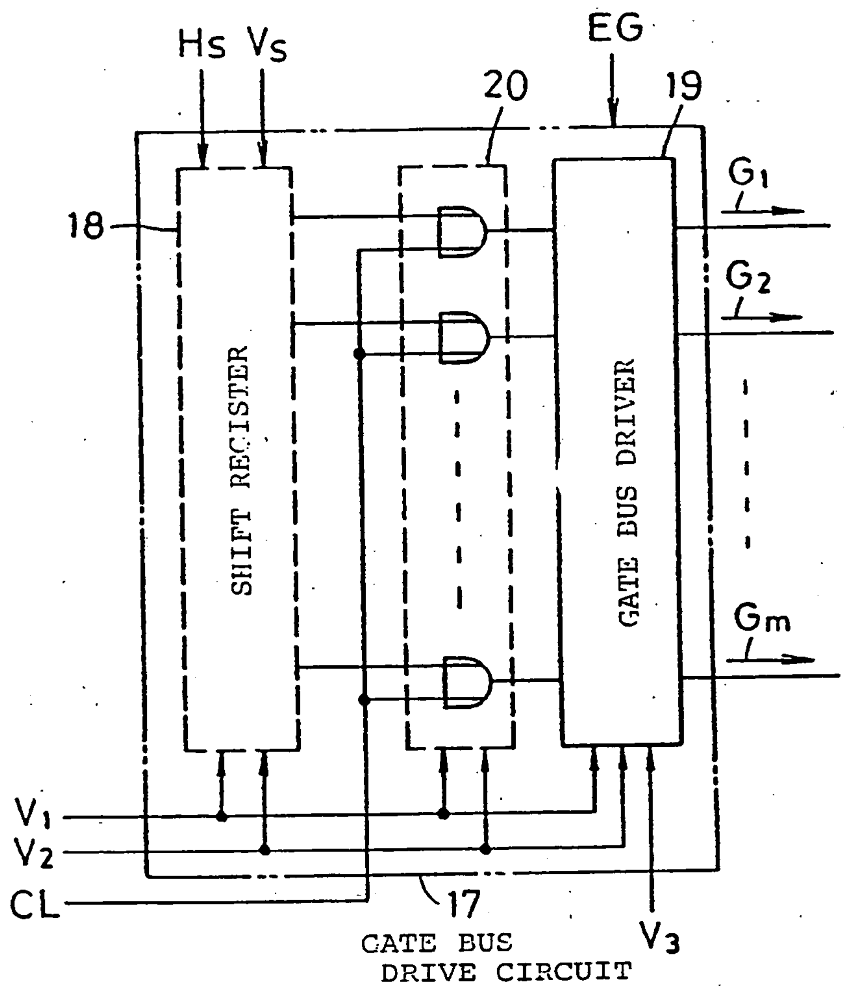

SOURCE BUS DRIVE CIRCUIT
16
E1
E2
E3
D
PCK
M
EG
Sn
S2
S1
14n
142
141
151
152
15m
12a
12b
12
13
10
G1
G2
Gm
GATE BUS DRIVER
19
17
18
Vs
Hs
CK D
P
Q
V1
V2
V3
CL
T

FIG. 4


Hs Vs
EG
20
19
18
SHIFT REGISTER
GATE BUS DRIVER
G1
G2
Gm
V1
V2
CL
17
V3
GATE BUS
DRIVE CIRCUIT

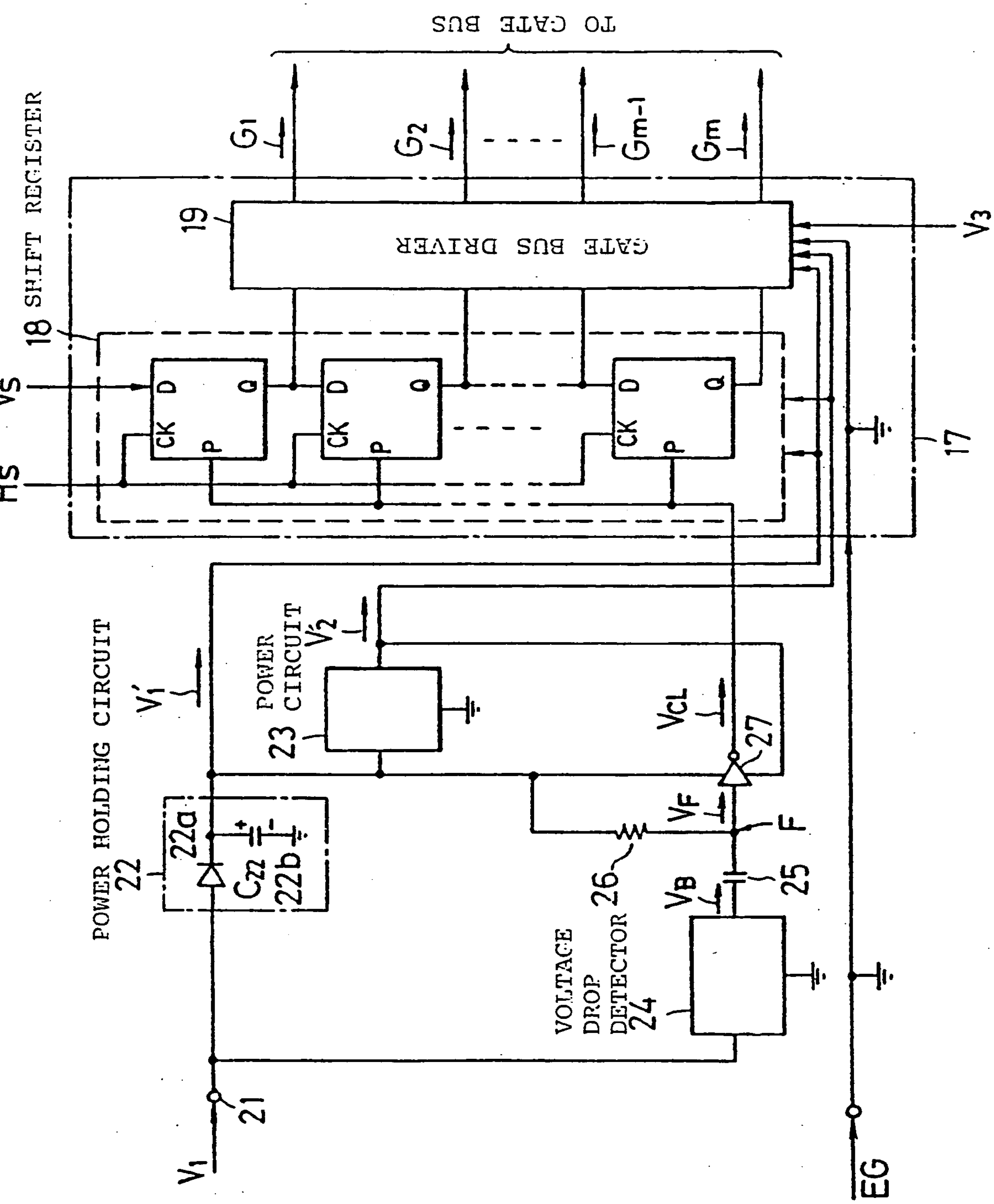
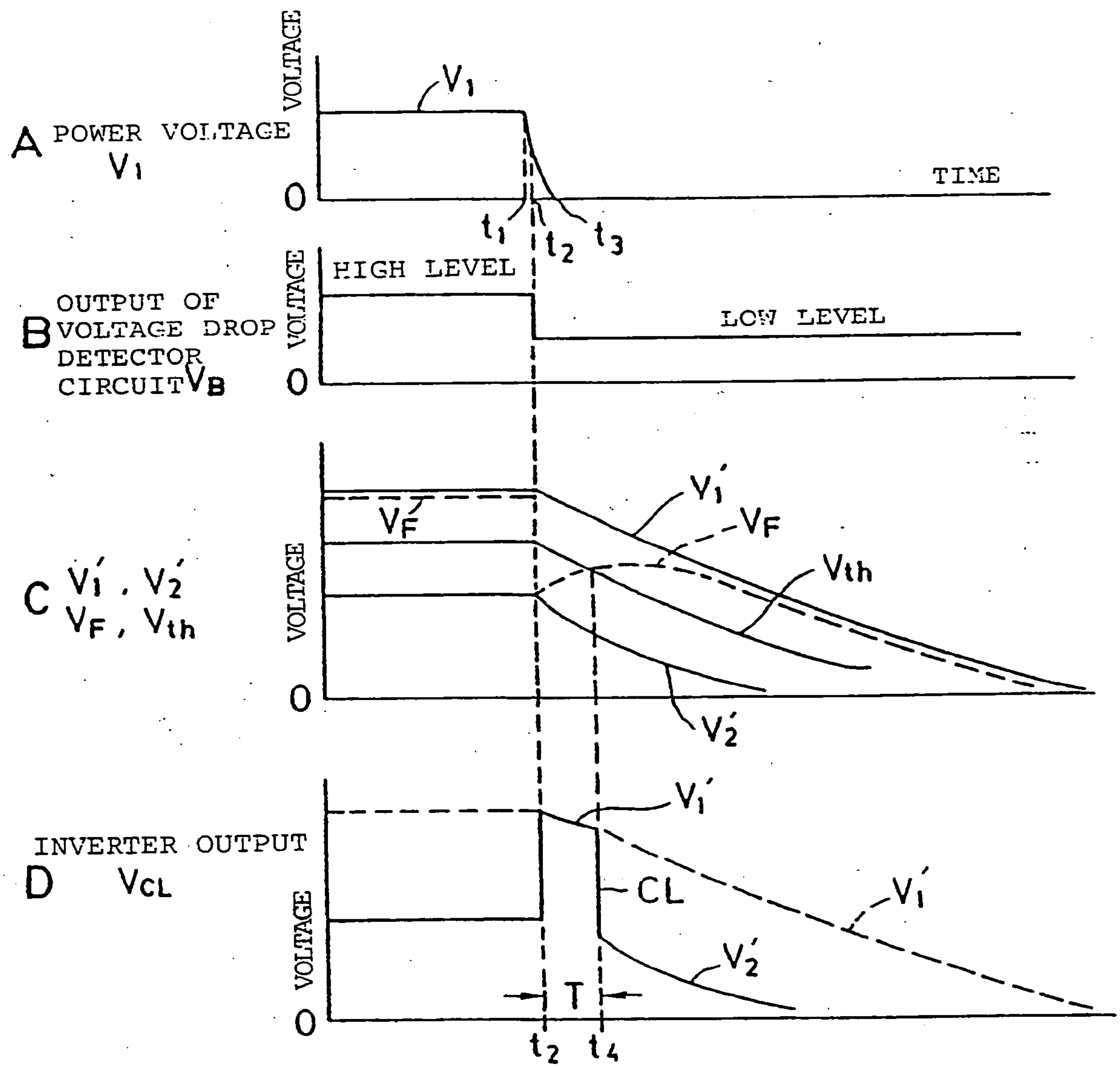

TO GATE BUS
SHIFT REGISTER
18
19
GATE BUS DRIVER
G_1
G_2
G_{m-1}
G_m
V_S
H_S
D
Q
CK
P
V_3
17
POWER HOLDING CIRCUIT
22
22a
22b
C_{22}
V_1'
POWER CIRCUIT
23
V_2'
V_{CL}
27
V_F
F
26
25
V_B
VOLTAGE DROP DETECTOR
24
V_1
21
EG

FIG. 5

FIG. 6


A POWER VOLTAGE V1
B OUTPUT OF VOLTAGE DROP DETECTOR CIRCUIT VB
C V1′, V2′ VF, Vth
D INVERTER OUTPUT VCL
VOLTAGE
TIME
HIGH LEVEL
LOW LEVEL
V1
V1′
V2′
VF
Vth
CL
T
t1
t2
t3
t4
0

INTERNATIONAL SEARCH REPORT

International Application No PCT/JP 88/01308

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl[4] G09G3/36

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
IPC	G09G3/36, G09G3/18

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

Jitsuyo Shinan Koho	1926 - 1987
Kokai Jitsuyo Shinan Koho	1971 - 1987

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category*	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	JP, A, 56-91297 (Citizen Watch Co., Ltd.) 24 July 1981 (24. 07. 81) Column 4 (Family: none)	1 - 7
Y	JP, A, 58-5792 (Hitachi, Ltd.) 13 January 1983 (13. 01. 83) Column 1 (Family: none)	1 - 7
Y	JP, U, 53-4853 (Matsushita Electric Works, Ltd.) 17 January 1978 (17. 01. 78) (Family: none)	2 - 7

* Special categories of cited documents:[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
February 8, 1989 (08. 02. 89)	February 20, 1989 (20. 02. 89)
International Searching Authority	**Signature of Authorized Officer**
Japanese Patent Office	